determining whether the cache memory is acting as the random access memory; and

assigning a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory.

17. (TWICE AMENDED) The computer according to claim 15, further comprising:

a bus control unit connecting the main memory and the cache memory;

a peripheral system connected to the computer through the bus control unit; and

an access control unit which accesses one of the main memory or the peripheral system instead of the cache memory when the cache memory is acting as the random access memory and an access request externally sent from an address outside the second address space of the cache memory is received.

Please **ADD** new claims 21 and 22 as follows:

21. (NEW) The method according to claim 13, wherein the computer includes a bus control unit connecting the main memory and the cache memory, and a peripheral system connected to the computer through the bus control unit, and wherein, when the cache memory is acting as the random access memory and an access request externally sent from an address outside the second address space of the cache memory is received, the computer accesses one of the main memory or the peripheral system instead of the cache memory.

22. (NEW) A computer including a main memory and a cache memory, the main memory having a first address space and the cache memory being capable of acting as a random access memory, comprising:

a determination unit which determines whether the cache memory is acting as the random access memory; and

an assignment unit which assigns a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory.